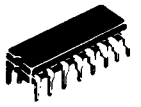
HM51258 Series

262144-word x 1-bit Static Column CMOS Dynamic RAM

The HM51258 is the 262,144 word by 1 bit static column dynamic random access memory utilizing the Hitachi 2μm CMOS process.
This device has static column circuit and it is good for high performance main storage or for page access applications.
While the row circuitry is still dynamic, and it controls the power consumed in the static circuitry. It realizes very low power dissipation.
Multiplexed address and the 16 pin pinout are compatible with the fully dynamic 256K DRAM HM50256.



(DP-16B)

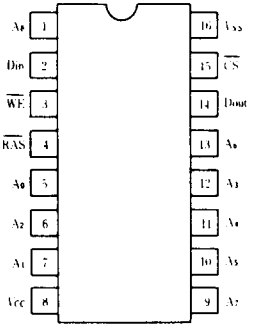
■ FEATURES

- 262,144 word x 1 bit SCRAM
- Double layer Poly-Si/Policide Process, high performance CMOS
- Power supply voltage 5V ± 10%
- Access time
  Row access time: 85/100/120/150ns
  Address access time: 40/45/55/70ns
- Cycle time
  Random Read&Write cycle time: 155/180/210/250ns
  Static Column cycle time: 45/50/60/75ns
- Lower power
  Standby: 11mW
  Active: 385/330/275/220mW
- Input and output: TTL compatible
- Refresh: 256 cycles/4ms
- Refresh function: $\overline{RAS}$ only refresh, $\overline{CS}$ before $\overline{RAS}$ refresh, Hidden refresh
- Static column mode capability
- Edge triggered write capability
- Fast $\overline{CS}$ output control

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM51258P-8	85ns	300 mil 16 pin Plastic DIP
HM51258P-10	100ns	
HM51258P-12	120ns	
HM51258P-15	150ns	

■PIN ARRANGEMENT

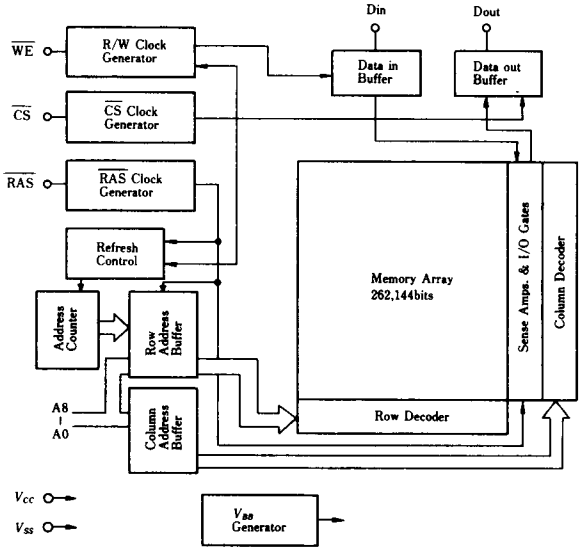


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A0–A8	Address inputs
$\overline{CS}$	Chip select
Din	Data in
Dout	Data out
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Read/Write input
Vcc	Power (+5V)
Vss	Ground
A0–A7	Refresh address inputs

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	−1.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=0 to +70°C)

Parameter	Sybmol	Test conditions	HM51258-8		HM51258-10		HM51258-12		HM51258-15		Unit	Note
			min	max	min	max	min	max	min	max		
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CS}$ Cycling; t_{RC}=min.	–	70	–	60	–	50	–	40	mA	1
Standby current	I_{CC2}	$\overline{RAS}$=V_{IH}, Dout=High Impedance	–	2	–	2	–	2	–	2	mA	
Refresh current	I_{CC3}	$\overline{RAS}$ only Refresh, t_{RC}=min	–	70	–	60	–	50	–	40	mA	
Standby current	I_{CC4}	$\overline{RAS}$=V_{IH}, Dout Enable	–	6	–	6	–	6	–	6	mA	1
Refresh current	I_{CC5}	$\overline{CS}$ before $\overline{RAS}$ Refresh, t_{RC}=min		60	–	55	–	45	–	35	mA	
Operating current	I_{CC6}	Static Column Mode, t_{RSC}, t_{WSC}=min		70	–	60	–	50	–	40	mA	1
Input leakage	I_{LI}	V_{in}=0 to 7V	−10	10	−10	10	−10	10	−10	10	μA	
Output leakage	I_{LO}	V_{out}=0 to 7V	−10	10	−10	10	−10	10	−10	10	μA	
Output high voltage	V_{OH}	I_{out}=−5mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{out}=4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	V	

Note) 1. I_{CC} depends on output loading condition when the device is selected.
I_{CC} max is specified at the output open condition.

■ CAPACITANCE (V_{CC}=5V±10%, T_a=25°C)

Parameter		Symbol	typ	max	Unit	Note
Input capacitance	Address, Data-In	C_{I1}	–	5	pF	1
	Clock	C_{I2}	–	7	pF	1
Output capacitance	Data-Out	C_O	–	7	pF	1, 2

Note) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (T_a=0 to +70°C, V_{CC}=5V±10%, V_{SS} = 0V)

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM51258-8		HM51258-10		HM51258-12		HM51258-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	155	–	180	–	210	–	250	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	–	70	–	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	55	10000	65	10000	75	10000	95	10000	ns	
$\overline{CS}$ Pulse Width	t_{CS}	25	–	25	–	30	–	35	–	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RCD}	20	60	25	75	25	90	30	115	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	45	20	55	20	65	25	80	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	–	25	–	30	–	35	–	ns	
$\overline{CS}$ Hold Time	t_{CSH}	85	–	100	–	120	–	150	–	ns	
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	10	–	ns	
Row Address Set-Up Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	10	–	15	–	15	–	20	–	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	–	4	–	4	–	4	–	4	ms	

• Read Cycle

Access Time from $\overline{RAS}$	t_{RAC}	–	85	–	100	–	120	–	150	ns	2, 3
Access Time from $\overline{CS}$	t_{CAC}	–	25	–	25	–	30	–	35	ns	3, 4
Access Time from Address	t_{AA}	–	40	–	45	–	55	–	70	ns	3,5,14
Column Address Hold Time to $\overline{RAS}$ on Read	t_{AR}	85	–	100	–	120	–	150	–	ns	
Read Command Set-Up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{CS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	–	45	–	55	–	70	–	ns	
$\overline{RAS}$ to Column Address Hold Time	t_{AH}	10	–	15	–	15	–	20	–	ns	16
Output Hold Time from Address	t_{OH}	5	–	5	–	5	–	5	–	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	0	35	ns	6

• Write Cycle

Column Address Set-Up Time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	15	–	20	–	25	–	30	–	ns	
Column Address Hold Time to $\overline{RAS}$ on Write	t_{AWR}	60	–	75	–	90	–	110	–	ns	
Write Command Set-Up Time	t_{WCS}	0	–	0	–	0	–	0	–	ns	10
Write Command Hold Time	t_{WCH}	20	–	25	–	30	–	35	–	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	65	–	80	–	95	–	115	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	30	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	–	25	–	30	–	35	–	ns	
Write Command to $\overline{CS}$ Lead Time	t_{CWL}	20	–	25	–	30	–	35	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	0	–	ns	11
Data-in Hold Time	t_{DH}	15	–	20	–	25	–	30	–	ns	10, 11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	60	–	75	–	90	–	110	–	ns	

(to be continued)

• Read-Modify-Write Cycle

Parameter	Symbol	HM51258-8		HM51258-10		HM51258-12		HM51258-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	180	–	210	–	245	–	290	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	–	100	–	120	–	150	–	ns	10
$\overline{CS}$ to $\overline{WE}$ Delay Time	t_{CWD}	20	–	25	–	30	–	35	–	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	–	45	–	55	–	70	–	ns	10
Output Hold Time from $\overline{WE}$	t_{OHW}	25	–	25	–	25	–	25	–	ns	

• Refresh Cycle

$\overline{CS}$ Set-up Time ($\overline{CS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	–	10	–	10	–	10	–	ns	
$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Hold Time	t_{RPC}	15	–	15	–	15	–	15	–	ns	

• SC Mode Cycle

SC Mode Cycle Time on Read	t_{RSC}	45	–	50	–	60	–	75	–	ns	
SC Mode Cycle Time on Write	t_{WSC}	45	–	50	–	60	–	75	–	ns	
$\overline{RAS}$ to Second $\overline{WE}$ Delay Time	t_{RSW}	90	–	105	–	125	–	155	–	ns	
SC Mode $\overline{RAS}$ Pulse Width	t_{RASC}	55	75000	65	75000	75	75000	95	75000	ns	
$\overline{CS}$ Precharge Time	t_{CP}	10	–	10	–	15	–	15	–	ns	
Write Invalid Time	t_{WI}	10	–	10	–	15	–	15	–	ns	

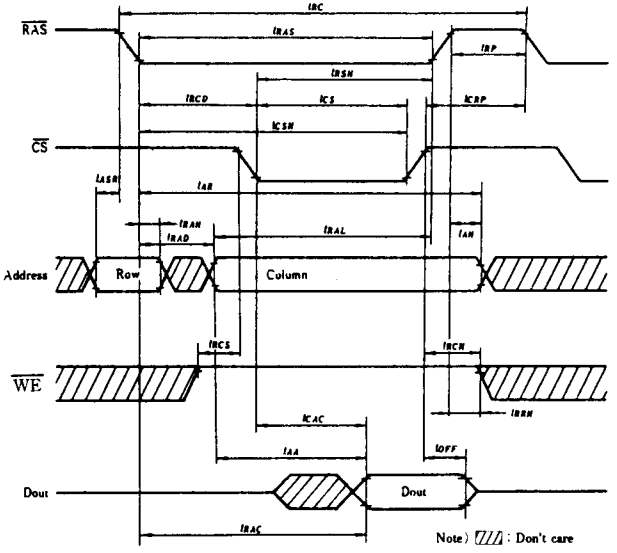
• SC Mode Read-Modify-Write and Mixed Cycle

SC Mode Cycle Time on Read-Write	t_{RWSC}	85	–	95	–	115	–	145	–	ns	12
Access Time from Previous $\overline{WE}$	t_{PWA}	–	80	–	90	–	110	–	140	ns	3, 13
Previous $\overline{WE}$ to Column Address Delay Time	t_{WAD}	20	40	25	45	30	55	35	70	ns	15
Column Address Hold Time to Previous $\overline{WE}$	t_{PWH}	80	–	90	–	110	–	140	–	ns	

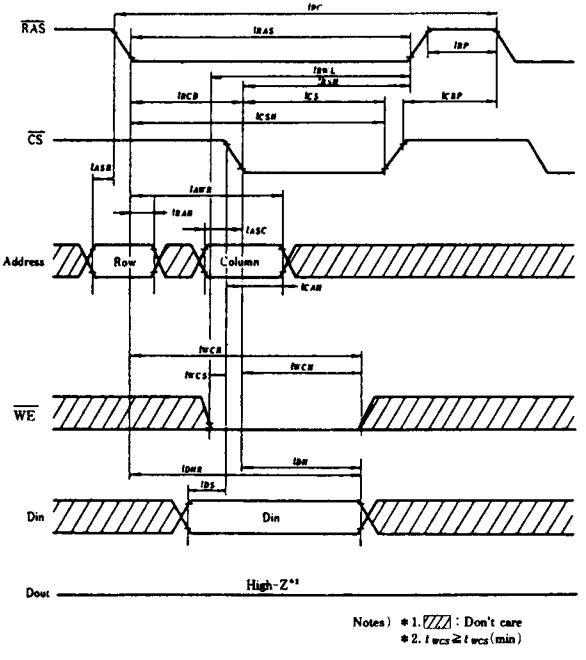
Notes:
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$(max) and $t_{RAD} \leqq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max) and $tRAD \leqq tRAD$ (max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$(max) and $t_{RAD} \geqq t_{RAD}$(max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$(min), $t_{CWD} \geqq t_{CWD}$(min) and $t_{AWD} \geqq t_{AWD}$(min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{RWSC}(min) = t_{AWD}(min) + t_{WAD}(max) + t_T
13. Assumes that $tWAD \leqq tWAD$(max). If $tWAD$ is greater than the maximum recommended value shown in this table, t_{PWA} exceeds the value shown.
14. Assumes that $t_{WAD} \geqq t_{WAD}$(max).
15. Operation with the t_{WAD}(max) limit insures that t_{PWA}(max) can be met, t_{WAD}(max) is specified as a reference point only, if t_{WAD} is greater than the specified t_{WAD}(max) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} is defined as the time at which the column address hold.
17. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
18. At least, 8 $\overline{CS}$ before $\overline{RAS}$ refresh cycle are required before using internal refresh counter.

■ TIMING WAVEFORMS

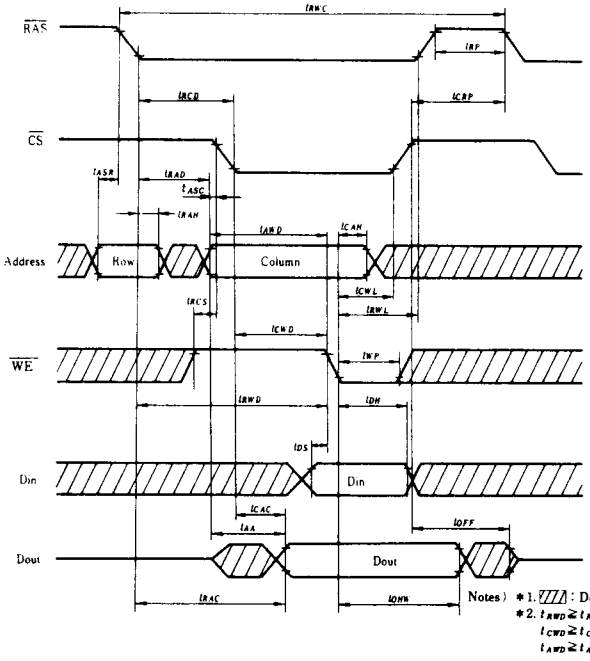
• Read Cycle



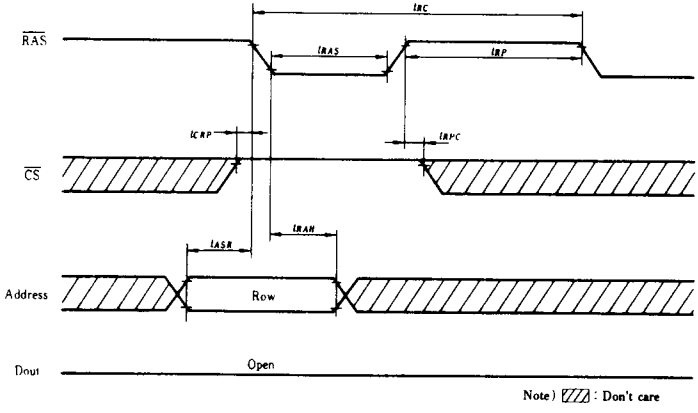
• Write Cycle



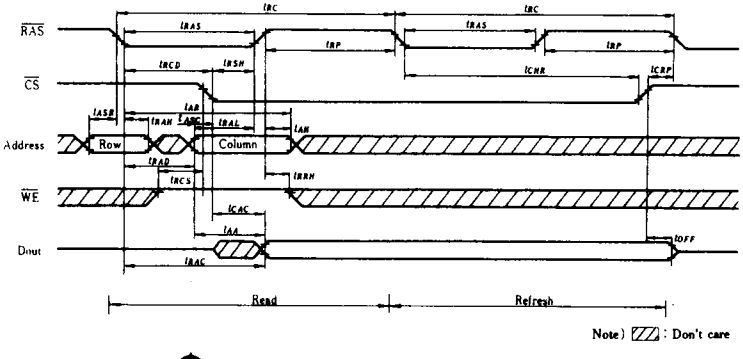
- **Read-Modify-Write Cycle**



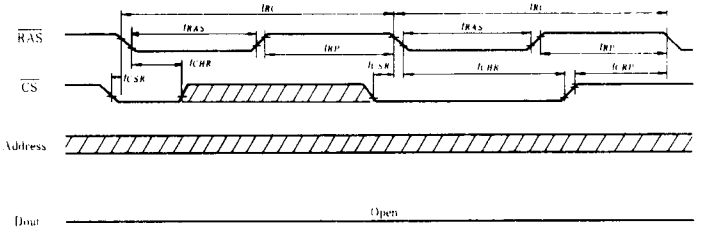
- **$\overline{RAS}$ Only Refresh Cycle**



- **Hidden Refresh Cycle**

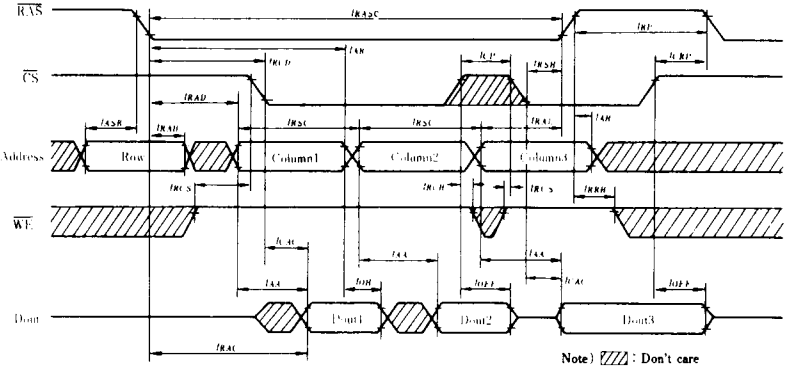


• $\overline{CS}$ before $\overline{RAS}$ Refresh Cycle



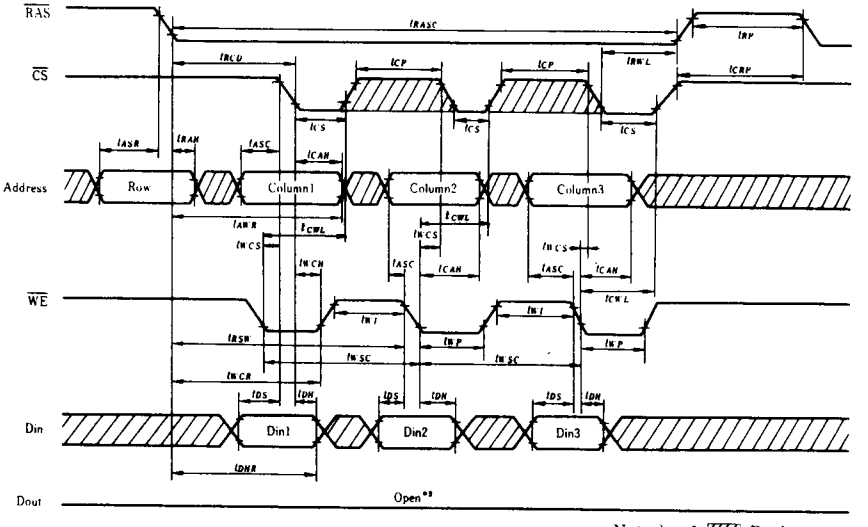
Note) ▨ : Don't care

• Static Column Mode Read Cycle



Note) ▨ : Don't care

• Static Column Mode Write Cycle



Notes) *1. ▨: Don't care
*2. $t_{WCS} \geq t_{WCS}$ (min)

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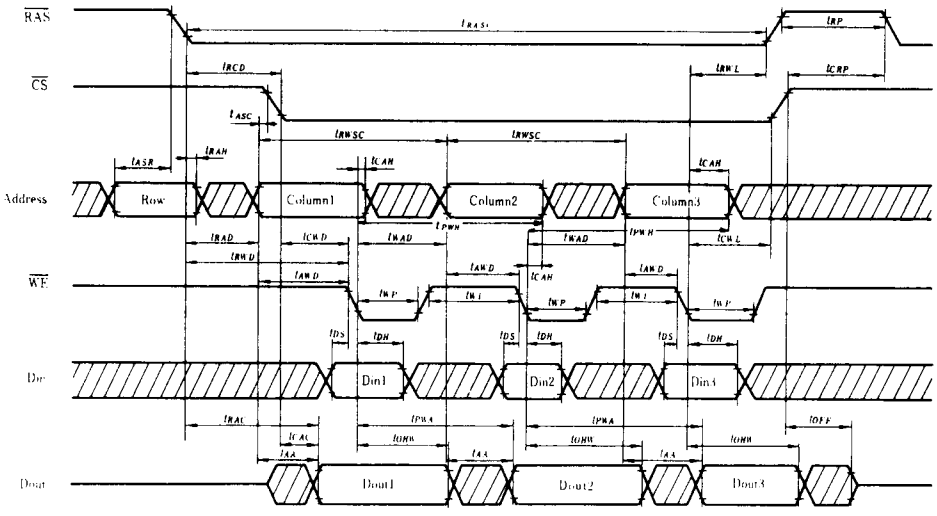
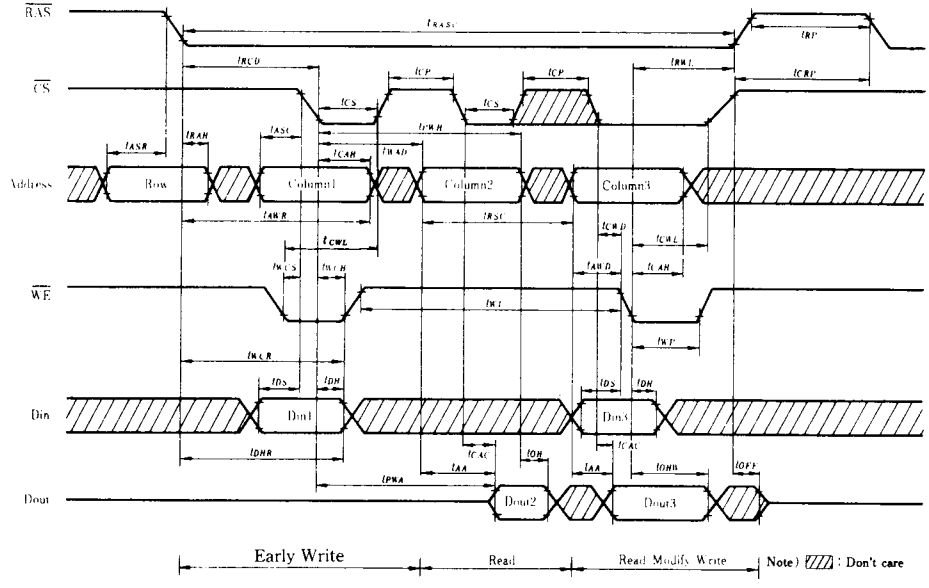
- **Static Column Mode Read-Modify-Write Cycle**

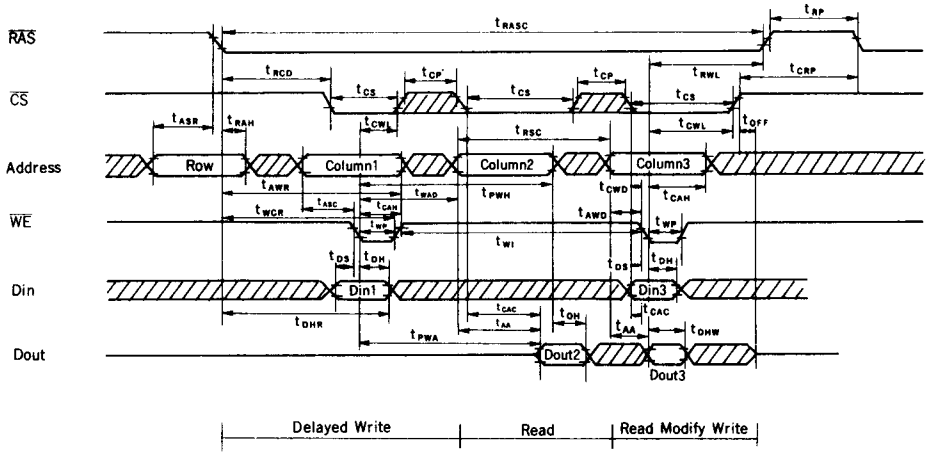


Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geq t_{RWD}$(min)
$t_{CWD} \geq t_{CWD}$(min)
$t_{AWD} \geq t_{AWD}$(min)

- **Static Column Mode Mixed Cycle-1**



- **Static Column Mode Mixed Cycle-2**



Note) ▨ : Don't care.